10/040852
12/28/01

U.S. UTILITY Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10040852 ~~10040864~~	12/27/01 ~~01/09/2002~~	~~430~~ 716	018	~~2822~~ 2875	DO

**APPLICANTS: Kasai Naoki;

**CONTINUING DATA VERIFIED:
THIS APPLICATION IS A DIV OF ~~09/703,867 11/02/2000 PAT 6,348,408~~

** FOREIGN APPLICATIONS VERIFIED:
~~JAPAN 11-314462 11/04/1999~~

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no	ATTORNEY DOCKET NO	
35 USC 119 conditions met	☐ yes ☐ no.	8013-1009-1	
Verified and Acknowledged Examiners's intials			

TITLE : Semiconductor device with reduced number of intermediate interconnection pattern and method of forming the same

U.S.DEPT. OF COMM./PAT.& TM:PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid		Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAMER	Primary Examiner	Application Examiner	
	PREPARED FOR ISSUE		

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